G2985

DDR Termination Regulator

Features

- **VIN Input Voltage Range: 2.5V to 5.5V**
- **VLDOIN Voltage Range: 1.1V to 3.5V**
- **Support DDR I (1.25 V_{TT}), DDR II (0.9 V_{TT}), DDR III (0.75 V_{TT}), DDR IIIL (0.675V_{TT}) and DDR IV (0.6 V_{TT}) Requirements**
- **Stable with Output Ceramic Capacitor**
- **PGOOD to Monitor Output Regulation**
- **EN Input for Shutdown Function (S3 Mode)**
- **Remote Sensing (VOSNS)**
- **2A Source and Sink Current**
- **±25mV Accuracy for VTT Refers to VTTREF**
- **±10mA Buffered Reference (VTTREF)**
- **Built-In Soft-Start and UVLO**
- **Over Current Protection**
- **Thermal Shutdown Protection**
- **TDFN3X3-10 (Thermal Pad) Package**

General Description

The G2985 is a linear regulator designed to meet the JEDEC SSTL (Series Stub Termination Logic) specifications in DDRI/II/III/IIIL/IV –SDRAM systems. It is designed for the system which has low input voltage, low cost, low noise and space consideration.

The G2985 provides accurate and fast response with up to 2A source/sink ability in load transient to track reference voltage with typically 20µF output capacitor. The terminated voltage can be generated by two external resistors or programmed by forcing REFIN pin at a desired voltage. Also the G2985 provides an open-drain PGOOD flag which monitors the output regulation and an EN signal to discharge VTT during STR (S3) mode.

Applications

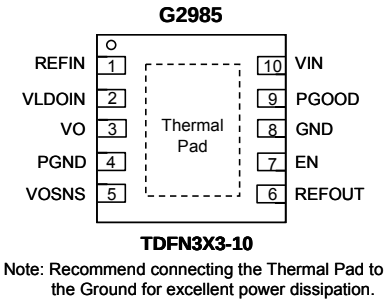
- **DDR I/II/III/IIIL/IV Memory Termination**
- **SSTL_3, SSTL_2, SSTL_18, SSTL_15**
- **HSTL Termination**
- **Notebook/Desktop/Server**
- **Telecom/Datacom, GSM Base Station, LCD-TV/PDP-TV, Copier/Printer, Set-Top Box**

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2985RE1D	2985	-40°C~85°C	TDFN3X3-10

Note: RE: TDFN3X3-10
1: Bonding code
D: Tape & Reel

Pin Configuration



TDFN3X3-10

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Typical Application